REMARKS

Claims 6, 10-12, 15 and 16 are pending. Amendment of claim 10 is proposed. A marked-up version showing the proposed changes is attached hereto as "**Version with markings to show changes made**."

Applicant gratefully acknowledges the indication that claims 6, 15 and 16 have been allowed. Favorable reconsideration of the rejection of claims 10-12 is earnestly solicited.

Claims 10-12 were rejected under 35 U.S.C. §102(e) as anticipated by Pan. Favorable reconsideration is earnestly solicited.

Pan describes a process for introducing hardening ions into the gate oxide film at the lateral edge parts thereof by way of ion implantation. Nitrogen or fluorine ions are used for this purpose, and Pan achieves suppressing of the hot carrier effect in an N-channel MOS-FET. In order to achieve the object, Pan uses an acceleration voltage of 5-50keV and a dose of $1 \times 10^{14} - 1 \times 10^{16}cm^{-2}$.

Contrary to Pan, the present invention achieves the ion implantation of N with a dose of $1 - 3 \times 10^{14}cm^{-2}$ as set forth in amended claim 10. By doing so, the problem of unwanted increase of surface state density, caused by the nitrogen atoms thus introduced at the interface between the oxide film and the silicon substrate, is successfully avoided.

In the case of Pan, on the contrary, there is caused extensive formation of surface states and the associated problem of gate leakage current or trapping of carriers because of the large dose of nitrogen ions at the time of the ion implantation process. Further, it is noted that the range of the

dose recited in claim 10 of the present invention is not insufficient for achieving the object of the invention of Pan of hardening the interface. As such, proposed amended claim 10 clearly distinguishes over Pan.

Further, it is noted that Pan uses the acceleration voltage of 5 - 50keV for achieving the desired hardening effect, while the use of such a large acceleration energy would also cause the problem of doping of the oxide/Si interface with N and associated problem of surface states.

Claim 11 specifies the energy range of not exceeding 10keV for the acceleration voltage. In fact, it is preferable to control the acceleration energy to be 1000eV or less at the time of the N ion implantation process in the present invention for avoiding formation of the surface states by the nitrogen ion penetrated deeply into the gate oxide film to the oxide/Si substrate interface region. Thus, the teaching of the present invention is entirely different from that of Pan.

For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicant would be desirable to place the application in better condition for allowance, the Examiner is encouraged to telephone applicant's undersigned attorney.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosure: Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/428,052

IN THE CLAIMS:

Claim 10 has been amended as follows:

10. (Six Times Amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate by a thermal oxide film;

forming a gate electrode pattern on said gate oxide film such that said gate electrode pattern is in direct contact with said gate oxide film;

forming diffusion regions in said substrate at both lateral sides of said gate electrode pattern by introducing impurity element into said substrate through said gate oxide film while using said gate electrode pattern as a mask; and

introducing N atoms, after said step of introducing said impurity element, into said gate oxide film while using said gate electrode pattern as a mask,

wherein said step of introducing N atoms into said gate oxide film includes an ion implantation process of N ions conducted with a dose of $1 - 3 \times 10^{14} cm^{-2}$.